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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,677	01/02/2004	Ko-Hsing Chang	12089-US-PA	1676

31561 7590 03/14/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
SOWARD, IDA M	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/707,677	CHANG ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed January 2, 2004.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7-11 and 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoo et al. (US 2003/0211689 A1).

In regard to claim 1, Yoo et al. teach a multi-level memory cell comprising: a substrate 100; a gate 175 disposed over the substrate100; a source region 210 and a drain region 210 configured in the substrate 100 on each side of the gate 175; and a bottom silicon oxide/silicon nitride/top silicon oxide layer 116, 155 & 165 disposed between the gate 175 and the substrate 100, wherein the top silicon oxide 165 has a first portion (the thinner section) and a second portion (the second portion of 165 being thick section above reference number 145) from the direction of the source region 210 to drain region 210, and the first portion has a thickness different from the second portion (Figure 10, pages 2 and 4-5, paragraphs [0024] and [0061]-[0067], respectively).

In regard to claim 2, Yoo et al. teach the cell further comprising a pair of spacers 200 disposed on each sidewall of the gate 175 (Figure 10, page 4, paragraph [0064]).

In regard to claim 3, Yoo et al. teach the cell further comprising lightly doped regions 190 disposed in the substrate 100 underneath the spacers 200 (Figure 10, page 5, paragraph [0066]).

In regard to claim 4, Yoo et al. teach material constituting the spacers 200 comprises silicon oxide (Figure 10, page 4, paragraph [0057]).

In regard to claim 7, Yoo et al. teach a multi-level memory cell, comprising: a substrate 100; a gate 175 disposed on the substrate 100; a source region 210 and a drain region 210 configured in the substrate 100 on each side of the gate 175; a tunneling dielectric layer 116 disposed between the gate 175 and the substrate 100; a charge-trapping layer 155 disposed between the tunneling dielectric layer 116 and the gate 175; and a top dielectric layer 165 disposed between the charge-trapping layer 155 and the gate 175, wherein the top dielectric layer 165 has at least two portions (the thin left hand section, the thick middle section and the thin right hand section) from the direction of the source region 210 to drain region 210, and each portion has different thickness (Figure 10, pages 2 and 4-5, paragraphs [0024] and [0061]-[0067], respectively).

In regard to claim 8, Yoo et al. teach material constituting the charge-trapping layer 165 comprises silicon nitride (Figure 10, page 2, paragraph [0024]).

In regard to claim 9, Yoo et al. teach the cell further comprising a pair of spacers 200 disposed on each sidewall of the gate 175 (Figure 10, page 4, paragraph [0064]).

In regard to claim 10, Yoo et al. teach the cell further comprising lightly doped regions 190 configured in the substrate 100 underneath the spacers 200 (Figure 10, page 5, paragraph [0066]).

In regard to claim 11, Yoo et al. teach material constituting the spacers 200 comprises silicon oxide (Figure 10, page 4, paragraph [0057]).

In regard to claim 14, Yoo et al. teach material constituting the tunneling dielectric layer 116 comprises silicon oxide (Figure 10, page 2, paragraph [0028]).

In regard to claim 15, Yoo et al. teach material constituting the top dielectric layer 165 comprises silicon oxide (Figure 10, page 2, paragraph [0024]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo et al. (US 2003/0211689 A1) as applied to claims 1-4, 7-11 and 14-15 above, and further in view of Reisinger (6,137,718).

Yoo et al. teach all mention in the rejection above. However, Yoo et al. fail to a bottom silicon oxide layer or tunneling dielectric layer having a thickness between about 20Å to 40Å, and a silicon nitride layer or charge-trapping layer having a thickness between about 40Å to 60Å.

In regard to claim 5, Reisinger teaches a bottom silicon oxide layer 51 having a thickness between about 30 Å to 60 Å, which is in the range of between about 20Å to 40Å (Figure 1, column 5, lines 36-55).

In regard to claim 6, Reisinger teaches a silicon nitride layer having a thickness of at least 50 Å, which is in the range of between about 40Å to 60Å (column 8, lines 54-55).

In regard to claim 12, Reisinger teaches a tunneling dielectric layer 51 having a thickness between about 30 Å to 60 Å, which is in the range of between about 20Å to 40Å (Figure 1, column 4-5, lines 19-22 and 36-55, respectively).

In regard to claim 13, Reisinger teaches charge-trapping layer having a thickness of at least 50 Å, which is in the range of between about 40Å to 60Å (columns 3 and 8, lines 40-42 and 54-55, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the multi-level memory cell structure as taught by Yoo et al. with the multi-level memory cell having silicon oxide layer or tunneling dielectric layer and silicon nitride layer or charge-trapping layer thickness as taught by Reisinger to increase storage density (abstract and column 2, lines 8-12).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to multi-level memory cells:

Chuang et al. (5,917,215)
Forbes (US 2004/0202032 A1)
Halliyal et al. (US 6,265,268 B1)
Lancaster et al. (5,774,400)
Lee et al. (US 6,858,906 B2)
Long et al. (US 6,225,669 B1)
Nakao (5,293,062)
Shin et al. (US 6,784,055 B2)
Takamura (US 2003/0218205 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
March 3, 2005